AMENDMENTS TO THE CLAIMS

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims

Claim 1 (Currently amended): A method of forming capacitors having geometric deep trenches, comprising:

providing a substrate;

forming a pad structure on the substrate;

forming a first hard mask layer on the substrate;

forming a patterned second hard mask layer on the first hard mask layer to expose a first opening;

forming a spacer layer in the first opening on the first hard mask layer to expose a second opening;

forming a third hard mask layer to fill the second opening;

removing the spacer layer to expose the first hard mask layer;

etching the first hard mask layer, with the second hard mask layer and the third hard mask layer acting as masks, to form a third opening with a salient of the first hard mask layer therein;

removing the second hard mask layer and the third hard mask layer; and

etching the first hard mask layer, the salient of the first hard mask layer, the pad structure, and the substrate to form a geometric deep trench in the substrate.

Claim 2 (Currently amended): The method as claimed in claim 1, after forming [[a]] the third hard mask layer to fill the second opening, further comprising subjecting the third hard mask layer to a flattening process to remove the third hard mask layer beyond the second opening.

Claim 3 (Currently amended): The method as claimed in claim [[1]] 2, wherein the flattening process is chemical mechanical polishing.

Claim 4 (Original): The method as claimed in claim 1, wherein the first hard mask layer is BPSG, AsSG, PSG, or BSG.

Claim 5 (Original): The method as claimed in claim 1, wherein the second hard mask layer is polysilicon or doped polysilicon.

Claim 6 (Currently amended): The method as claimed in claim 1, wherein the third hard mask layer and the ~~third~~ second hard mask layer are the same material.

Claim 7 (Original): The method as claimed in claim 1, wherein the spacer layer is dielectric material.

Claim 8 (Original): The method as claimed in claim 1, further comprising conformally forming the spacer layer with LPCVD, PECVD, HDPCVD, APCVD, or SACVD.

Claim 9 (Original): The method as claimed in claim 1, wherein the pad structure comprises a pad oxide layer and a pad nitride layer, and the steps of forming the pad structure comprise:

forming a pad oxide layer on the substrate; and

forming a pad nitride layer on the pad oxide layer.

Claim 10 (Original): The method as claimed in claim 1, wherein the process of forming the geometric deep trench in the substrate comprises:

etching the first hard mask layer, the salient of the first hard mask layer, and the substrate to remove the salient of the first hard mask layer completely to form a doughnut-shaped hollow in the substrate; and

etching the doughnut-shaped hollow of the substrate and the pad structure to form the geometric deep trench in the substrate.

Claim 11 (Currently amended): The method as claimed in claim 1, wherein the first hard mask layer is etched to form a residual first hard mask layer simultaneously, when the salient of the first hard mask layer is removed completely by ~~etchimg~~ etching.

Claim 12 (Currently amended): The method as claimed in claim 1, wherein ~~the~~ a width of the second opening is in inverse ratio to ~~the~~ a thickness of the spacer layer.

Claim 13 (Currently amended): The method as claimed in claim 12, wherein ~~the~~ a width of the salient of the first hard mask layer is in direct ratio to a width of the second opening.

Claim 14 (Currently amended): The method as claimed in claim 1, further comprising, after forming a geometric deep trench in the substrate, the steps of:

forming a buried plate in parts of the substrate of the geometric deep trench; and

forming a collar insulating layer and at least one conductive layer in the geometric deep trench.

Claim 15 (Currently amended): A method of forming capacitors having geometric deep trenches, comprising:

providing a substrate;

forming a pad structure on the substrate, comprising a pad oxide layer and a nitride layer formed on the substrate sequentially;

forming a first hard mask layer on the substrate;

forming a patterned second hard mask layer on the first hard mask layer to expose a first opening;

forming a spacer layer in the first opening on the first hard mask layer to expose a second opening;

forming a third hard mask layer to fill the second opening;

performing a flattening process to remove the third hard mask layer beyond the second opening [[.]];

removing the spacer layer to expose to the first hard mask layer;

etching the first hard mask layer, with the second hard mask layer and the third hard mask layer acting as masks, to form a third opening with a salient of the first hard mask layer therein;

removing the second hard mask layer and the third hard mask layer;

etching the first hard mask layer, the salient of the first hard mask layer, and the substrate to remove the salient of the first hard mask layer completely to form a doughnut-shaped hollow in the substrate; and

etching the doughnut-shaped hollow of the substrate and the pad structure to form ~~the~~ a geometric deep trench in the substrate.

Claim 16 (Original): The method as claimed in claim 15, wherein the flattening process is chemical mechanical polishing.

Claim 17 (Original): The method as claimed in claim 15, wherein formation of the pad oxide layer of the pad structure uses thermal oxidation.

Claim 18 (Original): The method as claimed in claim 15, wherein the first hard mask layer is BPSG, AsSG, PSG, or BSG.

Claim 19 (Original): The method as claimed in claim 15, wherein the second hard mask layer is polysilicon or doped polysilicon.

Claim 20 (Currently amended): The method as claimed in claim 15, wherein the third hard mask layer and the ~~third~~ second hard mask layer are the same material.

Claim 21 (Original): The method as claimed in claim 15, wherein the spacer layer is dielectric material.

Claim 22 (Original): The method as claimed in claim 15, wherein conformal formation of the spacer layer uses LPCVD, PECVD, HDPCVD, APCVD, or SACVD.

Claim 23 (Currently amended): The method as claimed in claim 15, wherein the first hard mask layer is etched to form a residual first hard mask layer simultaneously, when the salient of the first hard mask layer is removed completely by ~~etching~~ etching.

Claim 24 (Original): The method as claimed in claim 15, further comprising, after forming a geometric deep trench in the substrate:

forming a buried plate in parts of the substrate of the geometric deep trench; and

forming a collar insulating layer and at least one conductive layer in the geometric deep trench.